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Characterization and Modeling of Digital Circuits - Rohit Sharma 2018-06-11

This book provides a comprehensive overview of characterization techniques and advanced modeling of VLSI circuits for modern and advanced process nodes for timing, power, noise and variation models.

Intended audience includes research professionals, graduate students, circuit and PDK designers, characterization engineers, CAD developers, managers, mentors, and the merely curious. It is organized to serve as a compendium to a beginner, a ready reference to intermediate and source for an expert.

Digital Logic Design - Brian Holdsworth 2002-11-01

New, updated and expanded topics in the fourth edition include: EBCDIC, Grey code, practical applications of flip-flops, linear and shaft encoders, memory elements and FPGAs. The section on fault-finding has been expanded. A new chapter is dedicated to the interface between digital components and analog voltages. *A highly accessible, comprehensive and fully up to date digital systems text *A well known and respected text now revamped for current courses *Part of the Newnes suite of texts for HND/1st year modules

CMOS VLSI Design: A Circuits and Systems Perspective - Neil H. E. Weste 2011

The context of natural forest management and FSC certification in Brazil - Claudia Romero 2015-12-30

Management decisions on appropriate practices and policies regarding tropical forests often need to be made in spite of innumerable uncertainties and complexities. Among the uncertainties are the lack of formalization of lessons learned regarding the impacts of previous programs and projects. Beyond the challenges of generating the proper information on these impacts, there are other difficulties that relate with how to socialize the information and knowledge gained so that change is transformational and enduring. The main complexities lie in understanding the interactions of social-ecological systems at different scales and how they varied through time in response to policy and other processes. This volume is part of a broad research effort to develop an independent evaluation of certification impacts with stakeholder input, which focuses on FSC certification of natural tropical forests. More specifically, the evaluation program aims at building the evidence base of the empirical biophysical, social, economic, and policy effects that FSC certification of natural forest has had in Brazil as well as in other tropical countries. The contents of this volume highlight the opportunities and constraints that those responsible for managing natural forests for timber production have experienced in their efforts to improve their practices in Brazil. As such, the goal of the studies in this volume is to serve as the foundation to design an impact evaluation framework of the impacts of FSC certification of natural forests in a participatory manner with interested parties, from institutions and organizations, to communities and individuals.

The Pentium Chronicles - Robert P. Colwell 2006

Publisher Description

Elements of Programming Interviews - Adnan Aziz 2012-10-11

The core of EPI is a collection of over 300 problems with detailed solutions, including 100 figures, 250 tested programs, and 150 variants. The problems are representative of questions asked at the leading software companies. The book begins with a summary of the nontechnical aspects of interviewing, such as common mistakes, strategies for a great interview, perspectives from the other side of the table, tips on

negotiating the best offer, and a guide to the best ways to use EPI. The technical core of EPI is a sequence of chapters on basic and advanced data structures, searching, sorting, broad algorithmic principles, concurrency, and system design. Each chapter consists of a brief review, followed by a broad and thought-provoking series of problems. We include a summary of data structure, algorithm, and problem solving patterns.

The Algorithm Design Manual - Steven S Skiena 2009-04-05

This newly expanded and updated second edition of the best-selling classic continues to take the "mystery" out of designing algorithms, and analyzing their efficacy and efficiency. Expanding on the first edition, the book now serves as the primary textbook of choice for algorithm design courses while maintaining its status as the premier practical reference guide to algorithms for programmers, researchers, and students. The reader-friendly Algorithm Design Manual provides straightforward access to combinatorial algorithms technology, stressing design over analysis. The first part, Techniques, provides accessible instruction on methods for designing and analyzing computer algorithms. The second part, Resources, is intended for browsing and reference, and comprises the catalog of algorithmic resources, implementations and an extensive bibliography. NEW to the second edition: • Doubles the tutorial material and exercises over the first edition • Provides full online support for lecturers, and a completely updated and improved website component with lecture slides, audio and video • Contains a unique catalog identifying the 75 algorithmic problems that arise most often in practice, leading the reader down the right path to solve them • Includes several NEW "war stories" relating experiences from real-world applications • Provides up-to-date links leading to the very best algorithm implementations available in C, C++, and Java

Digital Circuit Fundamentals - Buck Engineering Co 1990

The Outsiders - S. E. Hinton 2019

The struggle of three brothers to stay together after their parent's death and their quest for identity among the conflicting values of their adolescent society.

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits - M. Bushnell 2006-04-11

The modern electronic testing has a forty year history. Test professionals hold some fairly large conferences and numerous workshops, have a journal, and there are over one hundred books on testing. Still, a full course on testing is offered only at a few universities, mostly by professors who have a research interest in this area. Apparently, most professors would not have taken a course on electronic testing when they were students. Other than the computer engineering curriculum being too crowded, the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook. For VLSI the foundation was provided by semiconductor device technology, circuit design, and electronic testing. In a computer engineering curriculum, therefore, it is necessary that foundations should be taught before applications. The field of VLSI has expanded to systems-on-a-chip, which include digital, memory, and mixed-signalsubsystems. To our knowledge this is the first textbook to cover all three types of electronic circuits. We have written this textbook for an undergraduate "foundations" course on electronic testing.

Obviously, it is too voluminous for a one-semester course and a teacher will have to select from the topics. We did not restrict such freedom because the selection may depend upon the individual expertise and interests. Besides, there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course. With equal tenacity, we address the needs of three other groups of readers.

VLSI Physical Design: From Graph Partitioning to Timing Closure - Andrew B. Kahng 2011-01-27

Design and optimization of integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. "VLSI Physical Design: From Graph Partitioning to Timing Closure" introduces and compares algorithms that are used during the physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

Low-Power Design and Power-Aware Verification - Progyna Khondkar 2017-10-05

Until now, there has been a lack of a complete knowledge base to fully comprehend Low power (LP) design and power aware (PA) verification techniques and methodologies and deploy them all together in a real design verification and implementation project. This book is a first approach to establishing a comprehensive PA knowledge base. LP design, PA verification, and Unified Power Format (UPF) or IEEE-1801 power format standards are no longer special features. These technologies and methodologies are now part of industry-standard design, verification, and implementation flows (DVIF). Almost every chip design today incorporates some kind of low power technique either through power management on chip, by dividing the design into different voltage areas and controlling the voltages, through PA dynamic and PA static verification, or their combination. The entire LP design and PA verification process involves thousands of techniques, tools, and methodologies, employed from the register transfer level (RTL) of design abstraction down to the synthesis or place-and-route levels of physical design. These techniques, tools, and methodologies are evolving everyday through the progression of design-verification complexity and more intelligent ways of handling that complexity by engineers, researchers, and corporate engineering policy makers.

Digital VLSI Systems Design - Seetharaman Ramachandran 2007-06-14

This book provides step-by-step guidance on how to design VLSI systems using Verilog. It shows the way to design systems that are device, vendor and technology independent. Coverage presents new material and theory as well as synthesis of recent work with complete Project Designs using industry standard CAD tools and FPGA boards. The reader is taken step by step through different designs, from implementing a single digital gate to a massive design consuming well over 100,000 gates. All the design codes developed in this book are Register Transfer Level (RTL) compliant and can be readily used or amended to suit new projects.

Static Timing Analysis for Nanometer Designs - J. Bhasker 2009-04-03

Timing, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the timing closure is the major milestone which dictates when a chip can be released to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis.

Unfortunately, there is no book currently available that can be used by a working engineer to get acquainted with the details of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing verification procedures and

techniques.

Formal Verification - Erik Seligman 2015-07-24

Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity. Learn formal verification algorithms to gain full coverage without exhaustive simulation Understand formal verification tools and how they differ from simulation tools Create instant test benches to gain insight into how models work and find initial bugs Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems

Low Power Design Methodologies - Jan M. Rabaey 2012-12-06

Low Power Design Methodologies presents the first in-depth coverage of all the layers of the design hierarchy, ranging from the technology, circuit, logic and architectural levels, up to the system layer. The book gives insight into the mechanisms of power dissipation in digital circuits and presents state of the art approaches to power reduction. Finally, it introduces a global view of low power design methodologies and how these are being captured in the latest design automation environments. The individual chapters are written by the leading researchers in the area, drawn from both industry and academia. Extensive references are included at the end of each chapter. Audience: A broad introduction for anyone interested in low power design. Can also be used as a text book for an advanced graduate class. A starting point for any aspiring researcher.

Implementing an InfoSphere Optim Data Growth Solution - Whei-Jen Chen 2011-11-09

Today, organizations face tremendous challenges with data explosion and information governance. InfoSphere™ Optim™ solutions solve the data growth problem at the source by managing the enterprise application data. The Optim Data Growth solutions are consistent, scalable solutions that include comprehensive capabilities for managing enterprise application data across applications, databases, operating systems, and hardware platforms. You can align the management of your enterprise application data with your business objectives to improve application service levels, lower costs, and mitigate risk. In this IBM® Redbooks® publication, we describe the IBM InfoSphere Optim Data Growth solutions and a methodology that provides implementation guidance from requirements analysis through deployment and administration planning. We also discuss various implementation topics including system architecture design, sizing, scalability, security, performance, and automation. This book is intended to provide various systems development professionals, Data Solution Architects, Data Administrators, Modelers, Data Analysts, Data Integrators, or anyone who has to analyze or integrate data structures, a broad understanding about IBM InfoSphere Optim Data Growth solutions. By being used in conjunction with the product manuals and online help, this book provides guidance about implementing an optimal solution for managing your enterprise application data.

Constraining Designs for Synthesis and Timing Analysis - Sridhar Gangadharan 2014-07-08

This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

Verilog HDL - Samir Palnitkar 2003

VERILOG HDL, Second Edition by Samir Palnitkar With a Foreword by Prabhu Goel Written for both experienced and new users, this book gives you broad coverage of VerilogHDL. The book stresses the practical design and verification perspective of Verilog rather than emphasizing only the language aspects.

The information presented is fully compliant with the IEEE 1364-2001 Verilog HDL standard. Among its many features, this edition-
• Describes state-of-the-art verification methodologies
• Provides full coverage of gate, dataflow (RTL), behavioral and switch modeling
• Introduces you to the Programming Language Interface (PLI)
• Describes logic synthesis methodologies
• Explains timing and delay simulation
• Discusses user-defined primitives
• Offers many practical modeling tips
Includes over 300 illustrations, examples, and exercises, and a Verilog resource list. Learning objectives and summaries are provided for each chapter. About the CD-ROM
The CD-ROM contains a Verilog simulator with a graphical user interface and the source code for the examples in the book. What people are saying about Verilog HDL- "Mr. Palnitkar illustrates how and why Verilog HDL is used to develop today's most complex digital designs. This book is valuable to both the novice and the experienced Verilog user. I highly recommend it to anyone exploring Verilog-based design." -Rajeev Madhavan, Chairman and CEO, Magma Design Automation
"This book is unique in its breadth of information on Verilog and Verilog-related topics. It is fully compliant with the IEEE 1364-2001 standard, contains all the information that you need on the basics, and devotes several chapters to advanced topics such as verification, PLI, synthesis and modeling techniques." -Michael McNamara, Chair, IEEE 1364-2001 Verilog Standards Organization
This has been my favorite Verilog book since I picked it up in college. It is the only book that covers practical Verilog. A must have for beginners and experts." -Berend Ozceri, Design Engineer, Cisco Systems, Inc.
"Simple, logical and well-organized material with plenty of illustrations, makes this an ideal textbook." -Arun K. Somani, Jerry R. Junkins Chair Professor, Department of Electrical and Computer Engineering, Iowa State University, Ames
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www.phptr.com ISBN: 0-13-044911-3

VLSI Interview Questions with Answers - Sam Sony 2012

If you can spare half an hour, then this ebook guarantees job search success with VLSI interview questions. Now you can ace all your interviews as you will access to the answers to the questions, which are most likely to be asked during VLSI interviews. You can do this completely risk free, as this book comes with 100% money back guarantee. To find out more details including what type of other questions book contains, please click on the BUY link.

Gyn/Ecology - Mary Daly 2016-07-26

This revised edition includes a New Intergalactic Introduction by the Author. Mary Daly's New Intergalactic Introduction explores her process as a Crafty Pirate on the Journey of Writing Gyn/Ecology and reveals the autobiographical context of this "Thunderbolt of Rage" that she first hurled against the patriarchs in 1979 and no hurls again in the Re-Surging Movement of Radical Feminism in the Be-Dazzling Nineties.

Low Power Methodology Manual - David Flynn 2007-07-31

This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches. In addition to providing a theoretical basis for these techniques, the book addresses the practical issues of implementing them in today's designs with today's tools.

Introduction to Logic Circuits & Logic Design with Verilog - Brock J. LaMeres 2019-04-10

This textbook for courses in Digital Systems Design introduces students to the fundamental hardware used in modern computers. Coverage includes both the classical approach to digital system design (i.e., pen and paper) in addition to the modern hardware description language (HDL) design approach (computer-based). Using this textbook enables readers to design digital systems using the modern HDL approach, but they have a broad foundation of knowledge of the underlying hardware and theory of their designs. This book is designed to match the way the material is actually taught in the classroom. Topics are presented in a manner which builds foundational knowledge before moving onto advanced topics. The author has designed the presentation with learning goals and assessment at its core. Each section addresses a specific learning outcome that the student should be able to "do" after its completion. The concept checks and exercise problems provide a rich set of assessment tools to measure student performance on each outcome.

Physical Design Automation of VLSI Systems - Bryan T. Preas 1988

Interview Questions and Answers - Richard McMunn 2013-05

VLSI Design - Esteban Tlelo-Cuautle 2012-01-20

This book provides some recent advances in design nanometer VLSI chips. The selected topics try to present some open problems and challenges with important topics ranging from design tools, new post-silicon devices, GPU-based parallel computing, emerging 3D integration, and antenna design. The book consists of two parts, with chapters such as: VLSI design for multi-sensor smart systems on a chip, Three-dimensional integrated circuits design for thousand-core processors, Parallel symbolic analysis of large analog circuits on GPU platforms, Algorithms for CAD tools VLSI design, A multilevel memetic algorithm for large SAT-encoded problems, etc.

The Image of the City - Kevin Lynch 1964-06-15

The classic work on the evaluation of city form. What does the city's form actually mean to the people who live there? What can the city planner do to make the city's image more vivid and memorable to the city dweller? To answer these questions, Mr. Lynch, supported by studies of Los Angeles, Boston, and Jersey City, formulates a new criterion—imageability—and shows its potential value as a guide for the building and rebuilding of cities. The wide scope of this study leads to an original and vital method for the evaluation of city form. The architect, the planner, and certainly the city dweller will all want to read this book.

Cracking Digital VLSI Verification Interview - Robin Garg 2016-03-13

How should I prepare for a Digital VLSI Verification Interview? What all topics do I need to know before I turn up for an interview? What all concepts do I need to brush up? What all resources do I have at my disposal for preparation? What does an Interviewer expect in an Interview? These are few questions almost all individuals ponder upon before an interview. If you have these questions in your mind, your search ends here as keeping these questions in their minds, authors have written this book that will act as a golden reference for candidates preparing for Digital VLSI Verification Interviews. Aim of this book is to enable the readers practice and grasp important concepts that are applicable to Digital VLSI Verification domain (and Interviews) through Question and Answer approach. To achieve this aim, authors have not restricted themselves just to the answer. While answering the questions in this book, authors have taken utmost care to explain underlying fundamentals and concepts. This book consists of 500+ questions covering wide range of topics that test fundamental concepts through problem statements (a common interview practice which the authors have seen over last several years). These questions and problem statements are spread across nine chapters and each chapter consists of questions to help readers brush-up, test, and hone fundamental concepts that form basis of Digital VLSI Verification. The scope of this book however, goes beyond technical concepts. Behavioral skills also form a critical part of working culture of any company. Hence, this book consists of a section that lists down behavioral interview questions as well. Topics covered in this book: 1. Digital Logic Design (Number Systems, Gates, Combinational, Sequential Circuits, State Machines, and other Design problems) 2. Computer Architecture (Processor Architecture, Caches, Memory Systems) 3. Programming (Basics, OOP, UNIX/Linux, C/C++, Perl) 4. Hardware Description Languages (Verilog, SystemVerilog) 5. Fundamentals of Verification (Verification Basics, Strategies, and Thinking problems) 6. Verification Methodologies (UVM, Formal, Power, Clocking, Coverage, Assertions) 7. Version Control Systems (CVS, GIT, SVN) 8. Logical Reasoning/Puzzles (Related to Digital Logic, General Reasoning, Lateral Thinking) 9. Non Technical and Behavioral Questions (Most commonly asked) In addition to technical and behavioral part, this book touches upon a typical interview process and gives a glimpse of latest interview trends. It also lists some general tips and Best-Known-Methods to enable the readers follow correct preparation approach from day-1 of their preparations. Knowing what an Interviewer looks for in an interviewee is always an icing on the cake as it helps a person prepare accordingly. Hence, authors of this book spoke to few leaders in the semiconductor industry and asked their personal views on "What do they look for while Interviewing candidates and how do they usually arrive at a decision if a candidate should be hired?". These leaders have been working in the industry from many-many years now and they have interviewed lots of candidates over past several years. Hear directly from these leaders as to what they look for in candidates before hiring them. Enjoy reading this book. Authors are open to your feedback. Please do provide your valuable comments, ratings, and reviews.

SystemVerilog for Verification - Chris Spear 2012-02-14

Based on the highly successful second edition, this extended edition of SystemVerilog for Verification: A

Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill. In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include: New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories, the test registry, and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.

Principles of VLSI RTL Design - Sanjay Churiwala 2011-05-04

Since register transfer level (RTL) design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc., all which are a function of the way the RTL was originally written. Readers will benefit from a highly practical approach to the fundamentals of these topics, and will be given clear guidance regarding necessary safeguards to observe during RTL design.

Substrate Noise - Edoardo Charbon 2007-05-08

In the past decade, substrate noise has had a constant and significant impact on the design of analog and mixed-signal integrated circuits. Only recently, with advances in chip miniaturization and innovative circuit design, has substrate noise begun to plague fully digital circuits as well. To combat the effects of substrate noise, heavily over-designed structures are generally adopted, thus seriously limiting the advantages of innovative technologies. Substrate Noise: Analysis and Optimization for IC Design addresses the main problems posed by substrate noise from both an IC and a CAD designer perspective. The effects of substrate noise on performance in digital, analog, and mixed-signal circuits are presented, along with the mechanisms underlying noise generation, injection, and transport. Popular solutions to the substrate noise problem and the trade-offs often debated by designers are extensively discussed. Non-traditional approaches as well as semi-automated techniques to combat substrate noise are also addressed. Substrate Noise: Analysis and Optimization for IC Design will be of interest to researchers and professionals interested in signal integrity, as well as to mixed signal and RF designers.

Digital Vlsi Design - Singh Ajay Kumar 2010-11-01

CMOS Logic Circuit Design - John P. Uyemura 2007-05-08

This is an up-to-date treatment of the analysis and design of CMOS integrated digital logic circuits. The self-contained book covers all of the important digital circuit design styles found in modern CMOS chips, emphasizing solving design problems using the various logic styles available in CMOS.

Static Timing Analysis Interview Questions with Answers - Sam Sony 2012

If you can spare half an hour, then this ebook guarantees job search success with STA interview questions. Now you can ace all your interviews as you will access to the answers to the questions, which are most likely to be asked during VLSI interviews. You can do this completely risk free, as this book comes with 100% money back guarantee. To find out more details including what type of other questions book contains, please click on the BUY link.

Vlsi High-speed I/O Circuits - Hongjiang Song 2010-02-01

This book is based on the class notes of a VLSI design course the author offered in Electrical Engineering Department at Arizona State University. The materials are organized into twenty-one special topics covering various aspects of analysis, modeling, and implementation of VLSI high-speed I/O circuits, such as prototype timing models, jitter analysis, transmitter, receiver, equalizer, phase-locked loop (PLL), and data

recovery circuit designs.

Verilog: Frequently Asked Questions - Shivakumar S. Chonnad 2007-05-08

The Verilog Hardware Description Language was first introduced in 1984. Over the 20 year history of Verilog, every Verilog engineer has developed his own personal "bag of tricks" for coding with Verilog. These tricks enable modeling or verifying designs more easily and more accurately. Developing this bag of tricks is often based on years of trial and error. Through experience, engineers learn that one specific coding style works best in some circumstances, while in another situation, a different coding style is best. As with any high-level language, Verilog often provides engineers several ways to accomplish a specific task. Wouldn't it be wonderful if an engineer first learning Verilog could start with another engineer's bag of tricks, without having to go through years of trial and error to decide which style is best for which circumstance? That is where this book becomes an invaluable resource. The book presents dozens of Verilog tricks of the trade on how to best use the Verilog HDL for modeling designs at various level of abstraction, and for writing test benches to verify designs. The book not only shows the correct ways of using Verilog for different situations, it also presents alternate styles, and discusses the pros and cons of these styles.

The Art of Timing Closure - Khosrow Golshan 2020-08-03

The Art of Timing Closure is written using a hands-on approach to describe advanced concepts and techniques using Multi-Mode Multi-Corner (MMMC) for an advanced ASIC design implementation. It focuses on the physical design, Static Timing Analysis (STA), formal and physical verification. The scripts in this book are based on Cadence® Encounter System™. However, if the reader uses a different EDA tool, that tool's commands are similar to those shown in this book. The topics covered are as follows: Data Structures Multi-Mode Multi-Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth, the author emphasizes short, clear descriptions which are implemented by references to authoritative manuscripts. It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design, and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise. This book is intended for anyone who is involved in ASIC design implementation -- starting from physical design to final design signoff. Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design.

VLSI Handbook - Norman Einspruch 2012-12-02

VLSI Handbook is a reference guide on very large scale integration (VLSI) microelectronics and its aspects such as circuits, fabrication, and systems applications. This handbook readily answers specific questions and presents a systematic compilation of information regarding the VLSI technology. There are a total of 52 chapters in this book and are grouped according to the fields of design, materials and processes, and examples of specific system applications. Some of the chapters under fields of design are design automation for integrated circuits and computer tools for integrated circuit design. For the materials and processes, there are many chapters that discuss this aspect. Some of them are manufacturing process technology for metal-oxide semiconductor (MOS) VLSI; MOS VLSI circuit technology; and facilities for VLSI circuit fabrication. Other concepts and materials discussed in the book are the use of silicon material in different processes of VLSI, nitrides, silicides, metallization, and plasma. This handbook is very useful to students of engineering and physics. Also, researchers (in physics and chemistry of materials and processes), device designers, and system designers can also benefit from this book.

A Collection of System Design Interview Questions - Antonio Gulli 2016-07-16

A collection of System Design Interview Questions

Cracking the Coding Interview - Gayle Laakmann McDowell 2011

Now in the 5th edition, Cracking the Coding Interview gives you the interview preparation you need to get the top software developer jobs. This book provides: 150 Programming Interview Questions and Solutions: From binary trees to binary search, this list of 150 questions includes the most common and most useful questions in data structures, algorithms, and knowledge based questions. 5 Algorithm Approaches: Stop being blind-sided by tough algorithm questions, and learn these five approaches to tackle the trickiest

problems. Behind the Scenes of the interview processes at Google, Amazon, Microsoft, Facebook, Yahoo, and Apple: Learn what really goes on during your interview day and how decisions get made. Ten Mistakes Candidates Make -- And How to Avoid Them: Don't lose your dream job by making these common mistakes.

Learn what many candidates do wrong, and how to avoid these issues. Steps to Prepare for Behavioral and Technical Questions: Stop meandering through an endless set of questions, while missing some of the most important preparation techniques. Follow these steps to more thoroughly prepare in less time.